

TSMC-02-120



January 5, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/687,183 10/16/03 |
Jung-Chih Tsao et al.
A NOVEL METHOD TO REDUCE Rs PATTERN
DEPENDENCE EFFECT
| _____ |

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on January 13, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 1/13/04

U.S. Patent 6,420,258 to Chen et al., "Selective Growth of Copper for Advanced Metallization," describes a selective growth of copper by an electrochemical method on a conformal seed layer in a trench.

U.S. Patent 6,228,771 to Allers, "Chemical Mechanical Polishing Process for Low Dishing of Metal Lines in Semiconductor Wafer Fabrication," describes a two step CMP process to minimize dishing of metal lines.

U.S. Patent 6,350,364 to Jang, "Method for Improvement of Planarity of Electroplated Copper," describes a copper deposition process that involves two electroplating steps.

U.S. Patent 6,225,223 to Liu et al., "Method to Eliminate Dishing of Copper Interconnects," describes a method of minimizing the amount of CMP dishing.

U.S. Patent 6,224,737 to Tsai et al., "Method for Improvement of Gap Filling Capability of Electrochemical Deposition of Copper," discloses a semiconductor structure having a trench formed therein.

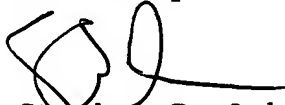
U.S. Patent 6,524,947 to Subramanian et al., "Slotted Trench Dual Inlaid Structure and Method of Forming Thereof," discusses a method of manufacturing a semiconductor structure.

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U.S. Patent 6,534,116 to Basol, "Plating Method and Apparatus that Creates a Differential Between Additive Disposed on a Top Surface and a Cavity Surface of a Workpiece Using an External Influence," discloses methods and apparatus for plating a conductive material on a substrate surface in a highly desirable manner.

U.S. Patent 5,674,787 to Zhao et al., "Selective Electroless Copper Deposited Interconnect Plug for USSI Applications," discusses an electroless plating process.

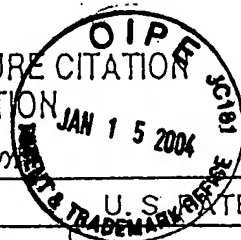
Sincerely,

A handwritten signature in black ink, appearing to be 'S. Ackerman', with a long horizontal stroke extending to the right.

Stephen B. Ackerman,
Reg. No. 37761

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)



Docket Number (Continued)

TSMC-03-120

Application Number

10/687,183

Applicant

Jung-Chih Tsao et al.

Filing Date

10/16/03

Group Art Unit

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	TITLE	CLASS	SUBCLASS	PRIOR DATE & APPROPRIATE
	6 2 2 8 7 7 1	5/8/01	Allers	438	692	3/23/00
	6 3 5 0 3 6 4	2/26/02	Jang	205	118	2/18/00
	6 2 2 5 2 2 3	5/1/01	Lin et al.	438	687	8/16/99
	6 2 2 4 7 3 7	5/1/01	Tsai et al.	205	123	8/19/99
	6 5 3 4 1 1 6	3/18/03	Basol	427	97	12/18/00
	6 5 2 4 9 4 7	2/25/03	Subramanian et al.	438	637	2/1/01
	6 4 2 0 2 5 8	7/16/02	Chen et al.	438	622	11/12/99
	5 6 7 4 7 8 7	10/7/97	Zhao et al.	437	230	1/16/96

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Portmox Pages, Etc.)

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.